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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/509,937	10/01/2004	Kazuya Taniguchi	2004-1548A	4957

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EXAMINER	
CRIBBS, MALCOLM D	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 06/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/509,937	TANIGUCHI ET AL.	
	Examiner	Art Unit	
	Malcolm D. Cribbs	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/09/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-10, *are presented for examination.*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki et al [US Patent No. 6,490,715] in view of Wong et al [US Patent No. 5,696,953] in further view of Conary et al [US Patent No. 5,842,029].

As per claims 1, and 10, Moriwaki et al teach the invention comprising:

a plurality of function blocks [Fig. 2, Blocks 121, and 122] that are supplied with power from a different one of a plurality of power supply circuits [Fig. 2, Circuits 111, and 112], respectively; and

a power supply control circuit for controlling the supply of power by the power supply circuits [Fig. 2, Circuit 101; Col 6 lines 43-49].

Moriwaki et al do not teach a system wherein a microcomputer is included as one of the plurality of blocks for controlling the supply of power. Specifically, Moriwaki et al

teach a method of controlling power supplied to function blocks contained on an integrated circuit by a control circuit. However, Moriwaki et al fail to detail one of the blocks being a microprocessor. A routineer in the art would have been motivated to look for a teaching for different possible types of the broad term used, blocks, to control power being supplied within an integrated circuit.

Wong et al teach another method of controlling power to blocks within an integrated circuit. Wong et al teach plural function blocks that are supplied with power and a microcomputer for controlling the supply of power to the plural function blocks [Col 5 lines 16-26; and Col 18 lines 50-61]. It is also obvious to one skilled in the art as submitted as prior art by the applicant [Applicants Admitted Prior Art, background art [AAPA]] that the plurality of blocks included within the integrated circuit consists of a microprocessor [AAPA Page 4 lines 4-11].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Moriwaki et al with Wong et al, which are analogous art, because they both teach a method of controlling power supplied to function blocks within an integrated circuit. Wong et al covers the deficiency of Moriwaki et al by including a microcomputer as one of the plurality of blocks to control power through power supply circuits instead using the conventional method of halting clocks.

As per claim 2, Wong et al do not teach halting the power to the microcomputer, within an integrated circuit, when predetermined data is received from the microcomputer. Specifically, Wong et al teach the halting of power to individual blocks when predetermined data is received from the microprocessor to reduce power consumption. However, Wong et al fail to detail the function of the microprocessor during a reduced power consumption mode. A routineer in the art would have been motivated to look for a teaching for the possible function of a microprocessor during a reduced power consumption mode.

Conary et al teach another reduced power consumption method for an integrated circuit [Col 4 line 49-51], wherein power is halted when predetermined data is received from the microprocessor. When the SRLPD, signal received by control circuit (930 Fig 9A) from processor to enter a reduced power consumption state, is asserted, control circuit 930 powers down the processor [Col 17 line 63 – Col 18 line 20]. In summary, Conary et al teach halting the power to the microprocessor, within the integrated circuit, to further reduce power being consumed.

It would have been obvious to one of ordinary skill in the art to combine the teachings of Moriwaki et al and Wong et al with Conary et al because they teach a method of reducing power consumption within an integrated circuit. Conary et al cover the deficiency of Moriwaki et al and Wong et al by teaching the detail of halting the

power to the microcomputer during a reduced power consumption mode instead of wasting power while remaining on.

As per claims 3 and 9, Conary et al teach the invention of the power supply control circuit includes a register for storing the interrupt signal, and the microcomputer operable to detect contents of the interrupt signal [Col 5 lines 31-44].

As per claim 4, Wong et al teach the invention of the power supply control circuit operable to output a power cutoff signal to the power supply circuits and the function blocks and the power supply control circuit each include an inter-block signal fixing circuit for fixing an input logic from a circuit to which supply of power is halted, at "L" or "H" level in accordance with the power cutoff signal [Col 19 lines 7-25].

As per claim 5, Wong et al teach the invention of the power supply control circuit operable to output a power cutoff signal to the power supply circuits, and the function blocks and the power supply control circuit each include an inter-block signal fixing circuit for fixing an output logic to a circuit that is in a state where the supply of power is halted, at "L" level in accordance with the power cutoff signal [Col 19 lines 7-25].

As per claim 6, Conary et al teach the invention of a storage unit which is always supplied with power and operable to retain system information while the supply

of power to the respective function blocks are halted [Col 17 line 65 – Col 18 line 14 control circuitry 930 is always supplied with power].

As per claim 7, Conary et al teach the invention of an input/output terminal circuit for giving and receiving a signal to/from outside, and the power supply control and the input/output terminal operate on power that is supplied from a common power supply circuit [Col 18 lines 1-4, wherein it would be obvious to a routineer in the art to include means for "receiving the appropriate power up request"].

As per claim 8, Wong et al teach the invention of the power supply control circuit operates on power that is supplied to the plural power supply circuits [Fig. 6A].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Malcolm D. Cribbs whose telephone number is 571-272-5689. The examiner can normally be reached on M-F 8AM-430PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Malcolm D Cribbs
Examiner
Art Unit 2115

June 7, 2006

CHUN CAO
PRIMARY EXAMINER